A Review of Thin Film Crystalline Silicon for Solar Cell Applications. Part 1 : Native Substrates.

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Abstract

Approximately half the cost of a finished crystalline silicon solar module is due to the silicon itself. Combining this fact with a high efficiency potential makes thin film crystalline silicon solar cells a growing research area. This paper, written in two parts, aims to outline world-wide research on this topic. The subject has been divided into techniques which use native substrates and techniques which use foreign substrates. Light trapping, vapour and liquid phase deposition techniques, cell fabrication and some general considerations are also discussed with reference to thin film cells.

Keywords

crystalline silicon, thin film, review

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1 Introduction

A major motivator for solar cell research and development is a reduction in cost of the finished module. To this end, thin film crystalline silicon cells are a promising candidate. Crystalline silicon has advantages of high efficiency potential, material abundance, a sharing of research and infrastructure costs with the integrated circuit industry, material non-toxicity and market dominance. Presently about half the cost of a finished module is due to the material itself, and around half of the silicon in a CZ ingot is lost as sawdust. The potential for cost reduction when using material which does not require dicing is therefore substantial. This review, of which this paper is part 1 of 2, discusses crystalline (single-, multi-, poly- and micro-crystalline) silicon cells which do not require dicing.

Although there are a diverse range of ways in which to achieve thin film silicon cells, most techniques require deposition or growth on a foreign or native substrate, optional recrystallisation and cell fabrication. Lift-off technologies also have a separation step which may fall before or after cell fabrication, and may mean the deposition or growth step is avoided. This paper first discusses the merits of various deposition techniques, cell fabrication on native substrates and light trapping techniques. The native substrates include ribbon growth, low cost silicon substrates and lift-off techniques. It is intended to be read in conjunction with a second paper which describes the state of research into deposition on foreign substrates, (both above and below the melting temperature of commercially available glass), cell fabrication techniques and cost considerations for thin film silicon cells.

Cell efficiencies depend strongly on the details of cell fabrication and are often a poor guide to fundamental material properties. A relatively poor material combined with a sophisticated cell processing sequence may result in a substantially higher cell efficiency than a better material with a rudimentary cell processing sequence. Open circuit voltage, V_{oc}, is often the best measure of overall material quality since it measures recombination rates, including bulk, grain boundary and surface recombination. However, for thin cells made from good quality material, where surface recombination is more important than bulk, the ranking of materials on the basis of V_{oc} is less certain.

2 Techniques Used for Silicon Deposition

Silicon can be deposited from the vapour or liquid phase. The main techniques used are chemical vapour deposition (CVD) and liquid phase epitaxy (LPE). LPE deposition only occurs on the exposed silicon surface and not on masked regions of the wafer or on parts of the epitaxy reactor, so there is the potential for high chemical yields. CVD deposition is difficult to mask and can also occur on the reactor walls, so the growth process must be optimised to ensure high chemical yields. Temperature ranges of 350–1000°C have been used with LPE, and growth rates up to 4μm/min have been achieved [1]. Processing temperatures for CVD range from a minimum of about 200°C (with PECVD) to a maximum of around 1200°C (with APCVD). Deposition rates range from about 10nm/min for LPCVD up to about 10μm/min for RTCVD [2]. CVD is a commonly used commercial process, but LPE has only been used commercially in some specialised applications such as for III-V crystals. Other deposition techniques which have been used to produce thin film silicon include ion-assisted deposition and sputtering.

2.1 LPE

LPE is capable of producing high quality layers. It has been found that mobilities in LPE layers are only slightly lower than those in similarly doped bulk Si [3]. Layers with high minority carrier lifetimes can be grown, so LPE layers are suitable for high efficiency solar cells. LPE is an attractive growth method because the layers are grown close to thermal equilibrium so they generally show a low density of structural defects and a low recombination activity at grain boundaries [4].

To make LPE commercially viable it is likely that growth rates and throughput will need to be increased. Rapid LPE has been pursued at the University of Konstanz [5]. A hole in the heating tube directly above the sample causes heat loss via radiation and therefore a strong temperature gradient at the substrate/growth interface. Growth rates of 2μm/min were achieved with a large tin melt for layers of 20–30μm with a resistivity of 1–2Ωcm. (Without the hole in the tube to cause the temperature gradient the growth rate was 0.2μm/min). Minority carrier diffusion lengths were 30–40μm if the furnace was unloaded directly after growth or 50–60μm if the furnace was cooled slowly before unloading. Self-supporting wafers have also been grown from a Si seed. The same apparatus has also been used to achieve high growth rates with an indium melt [1]. Strong temperature gradients, the large melt and sonic agitation of the melt resulted in growth rates of 2–4μm/min at 930°C. Layers on (100) sc-Si had a pyramidally textured surface. An efficiency of 4.5% was achieved on layers grown on heavily doped sc-Si substrates. There was a low V_{oc} due to low shunt resistance probably caused by shunting in the gaps between the pyramids.

It has been shown that LPE can be used to deposit silicon on large areas. Layers of fairly uniform thickness have been deposited on 5 inch wafers by LPE with a growth rate of 0.3–1μm/min [6]. An average minority carrier lifetime of 7μs was achieved over the whole of the epitaxial layer.

One of the features of LPE is that the incorporation of dopants depends on the temperature at which the layer is grown. Normally the thermodynamic driving force in LPE is the cooling of the melt, so LPE layers with a doping gradient and hence a drift field or pn-junction can be grown in one deposition step. At UNSW the Al content in a Sn/Al melt was adjusted to produce drift fields [7]. LPE can also be used to produce sharp dopant profiles (compared with diffusion which results in error-function doping profiles) by changing the growth solution after each layer [8]. Multilayers were grown at Max-Planck-Institut für Festkörperforschung using an LPE centrifuge to move solutions from one chamber to the next. Growth rates were 0.2–2μm/min.

Another implementation of LPE is the temperature difference method. The source is held at a higher temperature than the substrate to create a concentration gradient in the melt. Unlike conventional LPE, this is a steady state process and the temperature dependence of the element solubility does not affect the

layer composition. A temperature gradient of 10°C/cm allowed a growth rate of 0.3μm/min at Institut für Kristallzüchtung [9]. Layers grown on mc-Si had a roughness of 2–6μm for a layer thickness of 30μm, mostly from grooves at the grain boundaries. Lifetimes on layers grown on mc-Si were 5–10μs.

A comparison of Sn and In as solvents and Ga and Al as dopants for LPE has been made at UNSW using single crystal substrates [10] . A sliding LPE system was modified so that layers using two different solvents could be grown on one substrate. Better performances were obtained with In than with Sn and with Ga than with Al. It was found that layers grown with Sn solutions or doped with Al had reduced mobility and lifetime. However, at Institut National des Sciences Appliquées de Lyon, a Sn melt was used and the diffusion length was found to increase with the addition of Al and decrease with the addition of Ga [11]. A diffusion length of 280μm was achieved for an Al concentration of 0.9%.

2.2 CVD

CVD is a costly and complex method for deposition of silicon. The cost of precursor and dilutant gases used in a CVD process is substantial and a low cost process must minimise their use. The reasons for using CVD are that it is scaleable and high quality layers may be produced.

CVD of silicon occurs generally either in a mass transport or kinetically limited regime [12] [13] [14]. The mass transport regime occurs at higher temperatures and deposition is not as uniform, but a cold wall reactor design can be used. In a cold wall reactor the substrates are heated directly and as a result deposition takes place on the substrate, while the walls of the reactor, which are cooler, remain uncoated. This results in improved chemical yield. The kinetically limited regime occurs at lower temperatures and deposition uniformity is better. Temperature control is critical in the kinetically limted regime, so a hot wall reactor, which is essentially an isothermal furnace, is required.

With atmospheric pressure CVD (APCVD) the deposition is generally mass transport controlled, so wafers must be in a low packing density configuration to allow access of gases to the wafer surfaces. With low pressure CVD (LPCVD) deposition is kinetically controlled and wafers can be standing up, with a high packing density. This can lead to lower costs than with APCVD. However, deposition rates are generally lower. The degree of crystallinity obtained with LPCVD depends on the temperature. Films are fully crystalline at around 580–620°C; below this temperature range they are partly crystalline or amorphous [12] [15]. With LPCVD pressures in the range 1–100 Pa are used. Although the pressures used in LPCVD systems are three to four orders of magnitude lower than in APCVD systems, deposition rates are typically only one order of magnitude lower at similar temperatures. This is because the precursor gas is diluted in APCVD systems, so the partial pressures of the precursor gas differ by only an order of magnitude or so between APCVD and LPCVD systems.

Rapid thermal CVD (RTCVD) has been investigated at Fraunhofer ISE using an optically-heated APCVD system [2]. A special quartz wafer carrier is used which holds two layers of wafers and forms a volume separate from the rest of the reactor into which the precursor can be injected. This avoids deposition on the walls of the reactor and allows a high chemical yield. Chemical yields of 76% have been achieved with a growth rate of 4μm/min. Thickness and doping non-uniformities are about 10% over 15cm. The quality of the deposited layers has been demonstrated with the achievement of an efficiency of 17.6% on an epilayer deposited on a heavily doped Cz wafer with the RTCVD system.

LPCVD is a suitable technique to deposit thin-film silicon on foreign substrates because it produces large grain sizes [16] and can be used to coat large substrates [17] [18]. When polysilicon deposited by LPCVD is compared with polysilicon formed at low temperatures by plasma enhanced CVD (PECVD) and RF sputtering, the Hall mobility is higher and strain inside grains is lower [18]. Other advantages are the possibility for simultaneous deposition on a large number of substrates, uniformity, possibility of in-situ doping and that it leads to a low level of surface damage (compared with PECVD and sputtering) [17].

A disadvantage is that the material is highly defective, leading to low diffusion lengths [16]. In general, optical and electrical properties of in-situ doped LPCVD polysilicon are similar to those of polysilicon obtained by CVD and doped by implantation or thermal diffusion [19]. An increase in deposition time has been found to lead to an increase in both resisitivity and grain size [19].

A general feature of CVD is that it allows the fabrication of high quality layers. However, at low temperatures ($< 600°C$) the deposition rate is generally quite low [20]. The deposition rate can be scaled up by plasma activation of the precursor gas. With plasma enhanced CVD (PECVD) some of the energy required to break chemical bonds is provided by the plasma, so the temperature required to achieve a given growth rate can be lower. The high energy electrons in the plasma collide with and dissociate gas molecules which initiates the chemical reaction. In addition, bombardment of the wafer surface by positive ions from the plasma can change the surface chemistry, resulting in different film structures and growth rates. RF glow discharges, which result in weakly ionised plasmas, are most commonly used for PECVD. Depending on the reactor configuration, substrates are either within or downstream of the plasma. If the substrate is downstream of the plasma improved control of the reaction chemistry can be achieved but it is often only possible to deposit on one substrate at a time. A disadvantage of PECVD is that the plasma can cause surface damage during deposition [21]. When PECVD is performed at 200–300°C the result is relatively high quality Si. However, there is a high hydrogen content (10% atomic) [17]. This is a drawback in the process as bubbles appear in the film during the high temperature hydrogen evolution and this leads to macroscopic defect creation in the bulk. Low hydrogen content is beneficial to suppress spontaneous nucleation during depostion. Therefore, temperatures of about 500°C are used [17].

It has been found that plasma-induced damage by EBEP-CVD can be reduced by depositing at temperatures over 420°C or annealing at temperatures over 500°C, and avoided by making the electric potential of the substrate zero [22].

Electron Cyclotron Resonance CVD (ECRCVD) is a form of PECVD which uses ECR to produce the plasma. Cyclotron resonance occurs when the frequency of an alternating electric field matches the frequency of electrons orbiting the lines of force of a magnetic field. The plasma densities are higher with ECRCVD than those achieved with conventional RF PECVD [23]. A specific advantage of ECRCVD is that it causes relatively little layer damage since the plasma source and substrate are well separated, and the operation pressure and plasma potential are low [23] [24]. In addition, substrate biasing allows for separate variation of plasma current and particle energy; there is the possibility of in-situ substrate pre-treatment and layer post-treatment; there are no hot filaments or active electrodes; a higher proportion of the process gas is used; and there is the possibility for upscaling [24]. A limitation of ECRCVD is the need for very low pressure (0.1–1 Pa) and a high intensity magnetic field, which increases the cost of the system.

In Hot-Wire CVD (HWCVD) source gases such as SiH_4 and H_2 are pyrolytically decomposed on a filament catalyser which is heated to about 1300–2000°C and located several centimetres from the surface of the substrates. Gas-phase reactions and thin film deposition then take place from the atomic and molecular precursors generated at the filament surface. The process takes place under high vacuum (around 10 Pa). Doping can be readily achieved by adding a mixture of B_2H_6 or PH_3 into the source gas [25]. HWCVD is a simple and low cost proceedure [25] [26]. Single step fabrication of poly-Si [26] and reasonable deposition rates with good doping control are achievable [27] [28] [29]. Large area deposition is achievable by optimised superposition of precursors in a multiple filament configuration [28].

2.3 Recrystallisation

Once a silicon layer has been deposited, there are several improvements in quality which may be made by further crystallisation. The main high temperature recrystallisation technique is zone melting recrys-

tallisation (ZMR). Low temperature crystallisation techniques include laser crystallisation, solid phase crystallisation (SPC), rapid thermal processing (RTP) and vacuum and furnace annealing. Although crystallisation adds another step to the process, it allows the use of a lower cost, lower quality initial silicon deposition.

The advantages of using SPC of a-Si are that it is simple and cost effective, requires a low process temperature, produces a relatively high quality active layer, is easy to scale up [30] and allows the possibility of in-situ phosphorous doping [31]. SPC may be performed at temperatures above about 500°C, and produces large grain sizes. However, throughput is low [32]. Pulsed rapid thermal processing, PRTP, is a very fast method of SPC [33] as is aluminium-induced crystallisation (AIC), which is discussed in part 2 of this paper.

The grain size obtained with all random nucleation and growth crystallisation processes is inversely related to the nucleation rate [34]. The rapid temperature changes achievable with pulsed laser illumination allows nucleation to occur near the melting point of silicon without melting a glass substrate. Since the nucleation rate is low near the melting point of silicon, grain sizes obtained with laser crystallisation tend to be large.

For all growth temperatures and crystallisation techniques, there is generally a log-normal distribution of grain sizes [35]. The average grain size is a factor of 3–5 smaller than the maximum grain size. This is important because the because the open circuit voltage of a cell decreases significantly if even a small proportion of the grains have a diffusion length which is small compared to the rest of the grains in the cell.

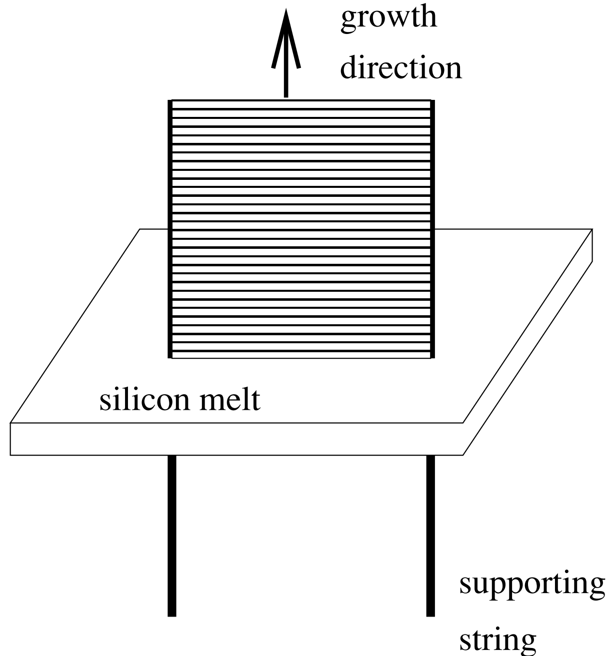

Figure 1: String ribbon growth, a form of vertical growth, after Wallace [36]

3 Ribbon growth

3.1 Introduction

Ribbon growth is a promising option for thin film silicon solar cells. Layers as thin as 5μm [36] [37] have been grown and cell efficiencies as high as 15.1% on 100μm multicrystalline layers [38] and 17.3% on single crystal layers demonstrated [39]. A large factor working in favour of ribbon grown silicon is that commercial viability has already been demonstrated [38] [40]. Ribbon growth has been included in this study because ribbon grown silicon does not require slicing. Although some of the ribbon growers are still producing thick layers, thinner layers are clearly a more economical option and research is moving in this direction.

3.2 Growth Techniques

Ribbon growth involves pulling a sheet of silicon from a molten stockpile. Solidification occurs at the meniscus and the meniscus geometry and pull rate determine both the rate and direction of cooling and the subsequent grain morphology [41]. Also included in this section are Silicon Sheets from Powder (SSP) whereby powdered silicon is irradiated to form sheets.

Ribbon growth can be divided into 2 broad categories [42]; vertical growth and horizontal growth. Vertical growth is much slower than horizontal growth. During vertical growth, the solidification front is perpendicular to the surface and crystallisation rates are measured in cm/min, leading to production rates in the range 10–160cm^2/min [42]. Examples of vertical growth techniques are dendritic web, edge-defined film-fed growth (EFG), string ribbon (see figure 1) and silicon sheet from powder (SSP). Kardauskas [40] claims that vertical growth has an inherent crystallisation rate limitation to 1–2cm/min due to the thermoelastic stress which produces both an increase in dislocation density and buckling. Vertical growth can be further classified into growth where the meniscus is short (in the order of the ribbon thickness) as in the case of EFG, and free rising meniscus (whereby the molten silicon has very little contact with the shaping element) as in dendritic web and string ribbon growth [41]. Slow growth produces substantially higher

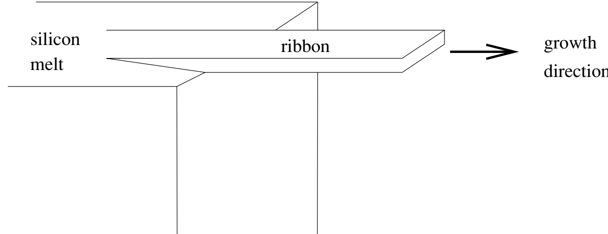

Figure 2: Horizontal ribbon growth, after Green [43]

quality silicon than fast growth, but this must be balanced against the higher production costs.

During horizontal growth, the solidification front is almost in the same plane as the ribbon surface and production rates of m^2/min may be achieved [42]. Fast growth has a large solid/liquid interface area which enables the latent heat of fusion to be more readily removed, therefore leading to higher growth rates [41]. Grain growth is parallel to the surface. Figure 2 shows a schematic of horizontal growth.

There are several groups which have had some success both in growing ribbon layers and in cell fabrication on ribbon grown silicon. A brief outline of the techniques used by some groups and the current status of ribbon and cell development is given below.

3.3 RGS - Bayer

Bayer fabricate the ribbon grown on substrate (RGS) material, which involves growth of molten silicon on a supporting substrate. Growth is fast, with a production rate of one $10\times10\text{cm}^2$ wafer/s [44]. Drawbacks are that material usage is high, layers are 300μm thick and the uneven front surface and carbon rich rear surface must be removed. This results in the removal of about 50μm of silicon from the front surface and 25μm from the rear.

Typical characteristics include a thickness of 300–400μm, a grain diameter of 0.1–0.5mm, a dislocation density of 10^5–$10^7/\text{cm}^2$, a carbon concentration of 1–$2\times10^{18}/\text{cm}^3$ and an oxygen concentration of $2\times10^{18}/\text{cm}^3$ [42]. Three different groups have made solar cells on this material. A comment relevant to all groups was that although the J_{sc} value was reasonable, V_{oc} was low. The results, as reported by Bayer [42] were : an efficiency of 11.1% and V_{oc} of 538mV by the University of Konstanz using slow cooled RGS, their V-grooving technique and hydrogen passivation, 10.1% by Fraunhofer ISE using rapidly cooled RGS and pre-gettering and 9.8% by ISFH, Emmerthal using slowly cooled RGS and standard MIS processing.

3.4 Dendritic web growth - GIT and EBARA Solar

Dendritic web growth is achieved by pulling dendrites of silicon from a solution of molten silicon, which becomes trapped between the dendrites and solidifies. The dendrites can be removed and recycled. The result is usually a bi-crystalline ribbon with twin boundaries at the centre where two mono crystals meet. The mono crystals are a result of single crystal growth from each edge of the solidifying meniscus. Grain growth is parallel to the surface [41]. Dendritic web growth is typified by low production rate, but high quality material [43].

Both the Georgia Institute of Technology (GIT) and EBARA Solar are involved in the production of dendritic web ribbons. Present production material from EBARA Solar is 100μm thick and 6cm wide, making cells of 10cm^2. A continual feeding process has allowed the growth of crystals of up to 37m in length [45]. A recent change has been from induction heating to resistance heating which has removed moving parts from the heating process, made the delivery of heat more flexible and increased the reproducibility [45].

In a collaboration between EBARA Solar and GIT, a single crystal silicon cell with an efficiency of 17.3% and a V_{oc} of 618mV has been demonstrated with a sophisticated cell processing sequence. The cell area was 4cm^2, and the material was 100μm thick [39]. This cell had a relatively high V_{oc} compared to other cells made on ribbon material which is due to high bulk lifetime and steps taken during cell processing to achieve a low surface recombination [39]. A high throughput RTP process was used to enable simultaneous diffusion of a light boron emitter and deep phosphorous BSF. The cell had a S_{eff} of 20cm/s and a bulk lifetime of 150μs. The modelling program PC1D-4 was used to show that the BSF resulted in a 4% increase in absolute efficiency compared to cells with infinite S_{eff} [39].

A new cell structure has been used on the 100μm thick ribbon and resulted in an efficiency of 14.4% (606mV) on a 4cm^2 cell. A pn junction was formed by alloying aluminium and n-type silicon. The junction is located at the rear of the cell and does not shunt. Contacts are screen printed [46].

EBARA Solar and GIT have been developing bifacial cells which have demonstrated almost equal rear and front surface efficiencies. An interdigitated back contact (IBC) cell has also been proposed. A precursor to this cell with front and rear contacts was made to check the use of an aluminium alloy p-n junction as a back junction. It was 4cm^2 and demonstrated an efficiency of 13.2% and a V_{oc} of 599mV [45].

3.5 String Ribbon - Evergreen Solar

String Ribbon is a growth technique used by Evergreen Solar. In the past it has also been called edge supported ribbon and edge stabilised ribbon. A non-conductive string is used to stabilise the edges of the ribbon and this remains in the material during cell fabrication [47]. Ribbon thickness is a function of melt temperature, ribbon thermal environment and pull speed. The main advantage of this method is a high tolerance of temperature variations; up to $\pm5°$C due to the high meniscus and edge stabilisation. A simple method of continuous melt replenishment has been developed and ribbon can be cut 'on the fly' [38].

Evergreen Solar have a manufacturing plant in operation 24 hours/day, 7 days/week which is using the string ribbon technique to produce material for commercial use in 30 or 60 W modules [38]. The ribbon is 300μm thick, 5.6cm wide and p-type with a resistivity of 1Ωcm [38]. Final cells are 15cm long, therefore having an area of 84cm^2 [47].

The issue of thermal stress has been addressed by both an active, tunable afterheater and a passive afterheater [36]. An active afterheater allowed growth rates of up to 25mm/min and a passive afterheater, 18mm/min (to produce 84cm^2 sheets [36]). The overall stress level was best lowered by having the largest cooling rate in regions of high temperature [37].

A 15.2% (581mV) cell has been demonstrated at Paul Scherrer Institut (PSI) using 200μm thick string ribbon. A RF plasma hydrogen passivation step and phosphorous and aluminium cogettering was used and together increased the minority carrier diffusion length by more than 100% [48].

In conjunction with Sandia National Laboratories and the University of New Mexico a 14.5% efficient cell with a V_{oc} of 600mV on 300μm thick ribbon has been demonstrated [49]. PECVD-nitride was used to simultaneously provide surface and bulk passivation and an anti reflection coating (ARC). H_2 and NH_3 plasma pretreatments have also been used both with and without a protective nitride layer. This resulted in lower efficiencies than the direct deposition method.

Evergreen Solar have been active in pursuing thin ribbon and have grown ribbons with thicknesses as low as 5μm [36] [37]. On a 100μm ribbon grown with a tunable afterheater, a 1cm^2 cell with an efficiency of 15.1% [38] has been manufactured. The V_{oc} of this cell was 599mV and the maximum V_{oc} seen using this method was 639mV on low resistivity material. The cell research was done at the Georgia Institute of Technology, using their SBLP (Simple BaseLine Process) which involves an Al BSF, hydrogen passivation and a double layer ARC [36].

Evergreen Solar have also worked in conjunction with GIT to increase the lifetime of the string ribbon

material. An increase of the as-grown value of 1μs to 9μs after cell fabrication has been achieved [50]. This is thought to be due to hydrogen passivation of defects and impurity gettering. Cell fabrication included a forming gas anneal (FGA) and phosphorous and aluminium gettering. The FGA resulted in an average increase in efficiency of 1.2%. The average cell results were a V_{oc} of 580mV and an efficiency of 14.6%. The best cell had an efficiency of 15.4% and a V_{oc} of 589mV. A 100μm thick cell which was fully screen printed and had a beltline diffused emitter (BLP) had an efficiency of 10.9% and a V_{oc} of 568mV. SiN was applied by PECVD as an ARC and front surface passivation. Further improvements may follow since the screen printing process possibly degraded the SiN and because there was poor back surface passivation [50].

Segregation of impurities has been found to occur naturally in the melt, leading to the possibility of using poorer quality material and/or periodic dumping of the melt.

3.6 EFG growth - ASE Americas

ASE Americas use the EFG technique to produce commercial quantities of string ribbon. EFG growth involves the movement of molten silicon up the interior of a graphite die by capillary action, after which it can be mechanically pulled [41]. Although the die provides edge stabilisation, it can also introduce impurities or react with the silicon to form silicon carbide precipitates. As the die dissolves, the width and thickness of the ribbon will increase [41]. Generally, EFG has few grain boundaries [51]. However it is also known to contain many dislocations, twin arrays, point defects and saturated carbon levels [51]. Kardauskas found the twin arrays to be of high density but mostly electrically inactive [40]. There is an inhomogeneous distribution of dislocations (often more than $10^6/cm^3$) and some regions have low diffusion lengths, which processing methods must take into consideration. Material tends to be of $\langle 110 \rangle$ orientation [51]. At ASE Americas, work has been done to increase yield and productivity by introducing continuous melt replenishment, using a shallow crucible with low melt volume and a short die and increasing the operation life of the die crucible.

ASE Americas produce 5m long, hollow, 8 sided tubes, each face being 10cm wide and 300μm thick. Routine production of cells with efficiencies around 14% has been demonstrated [40]. The tubes are cut with lasers to 10$\times$10cm. For the transfer from octagon to wafer, total material loss is around 8%. Following this, less than 5% of the material must be cleaned away before a cell can be made [40]. For more than 50 tubes 150–200kg of silicon goes through a single crucible and the residual silicon loss is about 500g [51]. Therefore, for the whole procedure, less than 13% of the input silicon is lost.

ASE Americas have grown cylinders with a thickness of 75–100μm. The as grown value of L_{diff} was 30–50μm and some grains sizes were 100μm. Iron was gettered only by aluminium alloying [51]. The advantages of cylindrical growth are faster pulling rates (by a factor of two), better electronic properties, reduction of thermoelastic stress due to the symmetry and the fact that rotation can be used to achieve a more uniform thickness. Future plans for the company include a 20MW production facility [51].

3.7 SSP - IMEC, KU Leuven and Fraunhofer ISE

A cooperation between groups at IMEC, KU Leuven and Fraunhofer ISE have grown silicon sheets from powder (SSP) by heating a compacted silicon powder on a substrate from one side with a halogen heat source. Some of the silicon powder (granular, of 0.15–1.5mm diameter) melts and 'percolates' into the underlying powder, combining with particles to form a self-supporting pre-ribbon. A zone melt recrystallisation process is then used to increase the grain size of this ribbon [52]. ZMR is typically done from both above and below the ribbon. Another alternative is to melt only from above. This simplifies the process, but grain sizes and growth rates are limited. Advantages of the SSP technique are that it is simple and that liquid silicon is not in contact with any sources of possible contamination [53]. Sheets are 350μm thick and 80$\times$150mm^2. Grains are typically several cm long and several mm wide and $\langle 221 \rangle$ orientation is

favoured. At Fraunhofer ISE, a cell of 13.1% (563mV) efficiency with a double layer ARC, has been made on these ribbons [53]. Recently, microwave remote plasma hydrogenation has been used on pre-ribbon substrates, for which the grain size is between 10–50μm, with the aim of fabricating cells on pre-ribbon. This has enabled increases in V_{oc} from 370mV to 500mV [52]. An additional Al BSF step further increased the V_{oc} value to 530mV, and a cell efficiency of 6.5% resulted [52]. A disadvantage of the SSP technique is that the ribbon is very thick, which means that lower quality silicon will probably be needed to reach a low cell cost.

3.8 SSP - University of Konstanz

Ribbons from powder on a stabilising substrate have been developed at the University of Konstanz. A resistively heated, movable graphite strip heater is used to irradiate the powder. The resulting poly-Si films have grain sizes in the order of several mm, are 20–800μm thick and are made from an original particle size of 0.3–125μm [54]. Minority carrier diffusion lengths of up to 20μm have been achieved. In contrast with the material produced at the Fraunhofer Institute, only a single irradiation is required. A disadvantage is that there are severe restrictions placed on substrate choice for thin ribbons relating to purity, wetting and separability.

Several different substrates have been used: quartz, quartz coated with Si_3N_4, graphite, graphite coated with SiC, graphite coated with PyroC, amorphous Carbon, pyroC, AlN, BN and BN coated with PyroC. A self-supporting silicon sheet has been achieved after separation from both quartz and pyrolytic graphite substrates. The pyrolytic graphite substrates gave a p-type Si with a diffusion length of about 20μm. Quartz produced only small grained silicon sheet [54].

As mentioned earlier, the University of Konstanz have also worked with the RGS mc-Si supplied by Bayer AG to form an 11.1% efficient cell with a V_{oc} of 538mV using microwave induced remote hydrogen plasma (MIRHP) (to passivate crystal defects) and V-grooving, a form of mechanical texturing [55]. The MIRHP step involves in-diffusion of atomic hydrogen. Greater efficiency is achieved with long passivation times at low temperature. However, there is the possibility of high temperature, short term passivation if it is done earlier in the process (before metalization) [55]. The optimum temperature and time are reported to be related to the concentration of interstitial oxygen which acts as an inhibitor for the atomic hydrogen. MIRHP was found to increase the efficiency by 1.1% absolute. Mechanical texturing developed due to the fact that anisotropic etching is not very effective on RGS material due to deviations from the (100) plane. It is a V-grooving technique which uses a dicing saw with bevelled sawing blades as a mechanical abasing device. The result is reduced reflectance and enhanced light trapping and therefore an increased charge carrier collection probability [55].

3.9 Summary of ribbon growth achievements.

Technique	Ribbon thickness	Efficiency, V_{oc}	Comment	Reference
RGS	300-400μm	11.1%, 538mV	cell by University of Konstanz	[42] [55]
RGS	300-400μm	10.1%	cell by Fraunhofer ISE	[42]
RGS	300-400μm	9.8%	cell by ISFH, Emmerthal	[42]
Dendritic Web	100μm	17.3% 618mV	single crystal	[39]
SSP (IMEC etc.)		13.1%, 563mV	on recrystallised ribbon	[53]
SSP (IMEC etc.)		6.5%, 530mV	on pre-ribbon	[52]
SSP (UK)	20–800μm		L_{diff} 20μm	[54]
EFG	300μm	14%	routinely achieved	[40]
EFG	75-100μm		cylindrical growth, L_{diff} 30–50μm	[51]
String Ribbon	300μm	14.5%, 600mV	PECVD as passivation and AR coating	[49]
String Ribbon	100μm	15.1%, 588mV	tunable afterheater	[38]
String Ribbon	5μm			[36] [37]
String Ribbon	100μm	10.9%, 568mV	screen printed with BLP	[50]
String Ribbon	200μm	15.2%, 581mV	cell by PSI	[48]

4 Silicon on low cost silicon

4.1 Considerations for Silicon on Silicon

Low cost silicon substrates have the advantage of thermal expansion coefficient matching and thermal stability. If a diffusion barrier is not used they also provide an epitaxial template allowing for the possibility of a high quality grown layer. Epitaxy allows a low interface defect density and therefore a low back surface recombination velocity. It is relatively easy to fabricate a heavily doped interface between the grown silicon layer and the silicon substrate, which further reduces rear surface recombination. A disadvantage of bare silicon substrates is that long wavelength, weakly absorbed light will be lost into the electrically inactive substrate.

There are two main approaches for growing silicon layers on silicon. One is to grow epitaxial layers on high-throughput silicon ribbons or upgraded metallurgical grade silicon (MG-Si). High efficiencies have been achieved on a model system of good quality multicrystalline substrates, but these have not yet been transferred to low-cost substrates.

Another approach is to use a barrier layer (most commonly SiO_2) to prevent diffusion of impurities from the substrate to the active layer. This produces grain sizes which are much smaller than those obtainable with a silicon epitaxial template. Recrystallisation is often used to overcome this hurdle, but it introduces extra costs. It is desirable that a diffusion barrier be reflective to long wavelength light and provide back surface passivation of the active layer.

The relative advantages of glass, opaque and multicrystalline silicon substrates has been considered by Blakers, using PC1D to model cells with the parameters expected to be achieveable on each type of substrate [56]. It was found that the optical advantage of glass relative to an opaque substrate is completely offset by lower quality electrical properties if the silicon grown on the opaque substrate has an effective diffusion length more than twice that of the silicon grown on glass.

4.2 Examples for Silicon on Silicon

4.2.1 High Efficiency Approaches

In order to develop deposition techniques and optimise growth parameters, silicon has been deposited on single crystal substrates by many groups. This enables some judgement to be made of the ultimate efficiency potential of each technique. Heavily-doped monocrystalline silicon is in some ways a model of a poor quality silicon material in that it is electrically inactive but does not have the complication of grain boundaries. High efficiencies have been achieved with epitaxial layers grown by both LPE and CVD.

When moderately-doped active layers are grown to above a critical thickness on heavily doped substrates (particularly boron doped substrates), misfit dislocations are generated. This is due to lattice mismatch caused by the differences in doping level. Experimental and numerical studies indicate that the recombination associated with these dislocations can limit V_{oc} to around 660mV [57]. These cells remain a useful model because most fabrication technologies will result in at least moderate back surface recomination.

The contribution of highly doped monocrystalline substrates to the efficiency of thin layers of active material on top has been investigated at Max-Planck-Institut für Festkörperforschung using PC1D and Sunrays [58]. For active layer widths of 20μm, substrates with doping of $6 \times 10^{18}/cm^3$ can contribute 4% to the short circuit current. For active layer widths of less than 10μm, the contribution to J_{sc} can be over 10%. For a thin layer cell with a high quality base and good front surface passivation, back diffusion of electrons into the substrate is important.

An early demonstration of this approach was at the Max-Planck-Institut für Festkörperforschung where

a V_{oc} of 663mV was achieved on a 20μm thick layer grown by LPE on a heavily doped substrate [59]. Later, an efficiency of 17.3% was demonstrated by CVD [60]. An efficiency of 15.4% has been achieved at ASE GmbH by CVD on heavily doped monocrystalline silicon substrates with no texturing but with a DLAR coating [61].

LPE layers on heavily doped c-Si substrates have been used to produce a cell with an efficiency of 14.7% and a V_{oc} of 659mV for a 16.8μm thick layer at Max-Planck-Institut für Festkörperforschung [62]. Effective diffusion lengths of up to 317μm have also been demonstrated on these layers.

The ANU has achieved an efficiency of 18.1% and V_{oc} of 666mV via LPE on a lightly doped c-Si substrate using an indium melt [63]. The epilayer was 35μm thick and the substrate was thinned to 15μm. Inverted pyramids were used to improve light trapping, while an oxide with boron diffused contact dots provided passivation of the rear of the cell. Al on top of the oxide acted as a rear reflector and electrical contact to the base. The measured value for J_{sc} included some contribution from the substrate because the substrate was lightly doped. A similar process yielded 17% on heavily doped sc-Si with most of the substrate removed [64].

An efficiency of 16.4% and a V_{oc} of 645mV has been achieved at UNSW on a 32μm thick layer with an area of 4cm^2 grown by LPE [65]. The substrate was heavily doped c-Si and a high-efficiency cell process was used including a microgrooved surface texture, a ZnS/MgF_2 DLAR coating on passivating oxide, and a graded doping level in the active layer.

A multilayer cell with an efficiency of 17.6% and V_{oc} of 664mV has been fabricated at UNSW with 5 active layers and a p^+ buffer layer, deposited by CVD on a heavily doped Cz substrate [66]. Microgrooved and inverted pyramid passivated emitter (PESC) structures were used. Deep isolating grooves were used to define the cell area. Only the uppermost two n-type layers were connected in parallel via the texturing process. The other n and p-type active layers were floating except for the rear p-type layer which was contacted via the p^+ buffer layer and the heavily-doped substrate.

Fraunhofer ISE have achieved an efficiency of 17.6% and a V_{oc} of 661mV with a high efficiency cell process on a layer grown by RTCVD on a heavily-doped Cz substrate [2]. The cell had an active layer thickness of 37μm plus a 15μm thick BSF. IMEC achieved an efficiency of 14.9% on a 30μm thick layer grown by CVD [57]. Beijing Solar Energy Research Institute has reached an efficiency of 12.1% on a 20μm thick active layer deposited on a sc-Si substrate by RTCVD [67].

The effect of substrate thinning for cells fabricated on heavily doped silicon substrates has been investigated at UNSW [68]. Substrate thinning can increase V_{oc} and FF by decreasing bulk recombination and hence the saturation current. Reflection of light from the thinned cell back surface can increase J_{sc}. MgF_2 between the silicon bulk and the aluminium contact can be used to reduce the metal/silicon contact area and therefore reduce rear surface recombination. Cells were thinned to a total thickness of less than 50μm. Thinning improved the efficiency of poorer cells by a factor of 23.7% [69]. The spectral response of thinned cells was much improved, especially at long wavelengths.

4.2.2 Silicon on Multi-crystalline Silicon

Good quality multicrystalline silicon (mc-Si) has been used as a model to develop techniques for depositing silicon on silicon. In mc-Si grain boundaries are present but grains are large and impurity levels are not as high as in metallurgical grade silicon. Currently the cost of high quality multicrystalline silicon is too high for it to be used commercially as a substrate, but metallurgical grade silicon and some forms of ribbon-grown silicon are commercially interesting.

Modelling with PC1D at ANU has shown that cells without light trapping can still have good efficiencies if diffusion lengths are relatively large (ie. corresponding to lifetimes $> 1\mu$s), which can be achieved on mc-Si substrates [70]. The same group has used LPE on mc-Si substrates to produce a cell of 15.4%

efficiency and V_{oc} of 639mV on a lightly doped substrate and a cell of 15.2% efficiency and V_{oc} of 639mV on a heavily doped substrate (with no texturing in either case, but with a TiO_2 ARC). It was estimated that the current originating from the lightly doped substrate was about 0.5mA/cm^2. Layers were grown 20–50μm thick. Periodic meltback was used to obtain much smoother morphology at the grain boundaries and thereby avoid emitter/substrate shunts.

A 13.3% efficient cell with a V_{oc} of 615mV has been fabricated at IMEC and KU Leuven on a 20μm thick active layer grown by APCVD on a highly-doped mc-Si substrate [71]. The cell process included an ARC but had no other light confinement. It was found that the optimal resistivity for the active layer is about 0.2Ωcm since a higher resistivity increases the grain boundary barrier height. Microwave induced remote plasma (MIRP) hydrogenation increased the diffusion length from 19μm to 29μm. The back surface recombination velocity at the interface between the highly-doped substrate and the active layer was about 3×10^3cm/s.

Screenprinting and laser grooved buried grid processes have been applied to epilayers grown on mc-Si substrates in a collaboration between IMEC and BP Solar [72]. Layers were grown by APCVD to a thickness of 20μm at a growth rate of 5μm/min. A resistivity of 0.2Ωcm was achieved to a depth of 15μm. In the remaining 5μm, the resistivity was lowered due to indiffusion of dopants from the heavily doped mc-Si substrate. Indiffusion of dopants from the substrate reduces the active cell volume and hence increases V_{oc}. The short circuit current tends to increase due to the BSF effect, but tends to decrease due to the reduction in cell volume, so there is an optimum depth of indiffusion. The BSF due to the indiffusion also reduces the sensitivity of the cell to recombination at the substrate/epilayer interface. It was found that epitaxy induced a surface texture due to development of $\langle 111 \rangle$ facets on the grown layers. The texture resulted in a difference in J_{sc} of 2.4mA/cm^2 between the textured cell and a non-textured cell simulated with PC1D. An efficiency of 13.2% was achieved on a 20μm thick epilayer grown on a V-grooved mc-Si substrate. An industrial-type process was used which included $POCl_3$ emitter diffusion, PECVD nitride deposition, screenprinted metallization, firing through nitride, parasitic junction removal and evaporation of MgF_2. This process resulted in an efficiency of 11% on an epilayer grown on a non-textured, heavily doped EFG ribbon substrate. It has been found that the level of hydrogen passivation achieved with firing through nitride is not as high as that produced with microwave induced remote plasma (MIRP) hydrogenation [73]. Firing through nitride is attractive industrially because it is a much quicker process than MIRP hydrogenation.

A collaboration between Georgia Institute of Technology, Astropower, Sandia National Laboratories and EBARA Solar Inc has investigated rapid thermal process (RPT) of various silicon substrates [74]. Efficiencies of 17.1%, 16.6%, 15.1% and 11.6% have been achieved on FZ, Cz, dendritic web and polycrystalline Silicon-Film^{TM} respectively without any conventional furnace processing steps. The process involves rapid, simultaneous emitter and BSF diffusion followed by rapid, low temperature deposition of a PECVD SiN/SiO_2 DLAR coating. The trapped hydrogen in the SiN layer is used to passivate bulk and surface defects. Slow cooling, rather than quenching during the rapid thermal anneal, improved the relative efficiencies of dendritic web and Silicon-Film cells by 50% and 15% respectively due to an increase in bulk lifetime. With slow cooling the process time for the emitter and BSF diffusion was up to 12 minutes.

LPE on MG-Si substrates with a Cu/Al solvent has been investigated at NREL [75]. A diffusion length of 42μm has been achieved for a layer thickness of 30μm on a MG-Si substrate. LPE often takes place in a H_2 atmosphere to remove native oxide from the silicon but in this case an Ar atmosphere was used and the Al performs the native oxide removal. The Cu was found to reduce Al incorporation into grown layers. An advantage of this approach is the rather high Si solubility in the Al/Cu solvent of 20–35 at%. This high silicon concentration has been found to result in more isotropic growth rates on grains of different orientations than solvents with lower Si solubilities, such as In or Sn, and also offers the potential for

higher deposition rates. Resistivities of up to 0.2Ωcm were achieved with Cu levels below the threshold for solar cell degradation [76].

Epitaxial layers have been grown on heavily doped RGS-ribbon substrates by CVD in a collaboration between IMEC, KU Leuven and Bayer AG [77]. RGS silicon has a high dislocation density of 10^8cm^{-2} and a surface roughness of 100μm (+/- 50μm) in a 400 micron thick ribbon. No initial polishing steps to make the ribbons smoother were undertaken. The epitaxial layers had grain sizes of 10–100μm and a defect density of 10^6–10^7cm^{-2}. A cell efficiency of 10.4% and a V_{oc} of 558mV were achieved on a 30μm thick layer with an area of 25cm^2. The cell process included aluminium gettering of the substrates and passivation of the active layer bulk by microwave induced remote plasma hydrogenation. Diffusion lengths were 15–20μm after hydrogenation.

LPE has been used to grow layers on heavily doped RGS ribbons in a collaboration between Institut für Kristallzüchtung, Max-Planck-Institut für Festkörperforschung and Universität Erlangen [78]. A slider system was used with an In solvent, a cooling rate of 0.7°C/min and a temperature range of 950–850°C which gave a thickness of about 20μm. The substrate was mechanically polished to reduce the roughness of the RGS substrate. Despite this, the epilayer had a roughness of about 20μm ie. same order as layer thickness. Cells were fabricated but were found to be shunted due to contact of the emitter to the p^+ RGS substrate at dips in the epilayer.

Silicon Sheets from Powder (SSP) is a ribbon material with an average grain size of 60μm and a dislocation density of 10^6–10^7cm^{-2}. The ribbons have a surface roughness of 200μm over 5m. This can affect the width of grid fingers (according to whether they were close to the mask or not). Epitaxial layers have been grown on SSP ribbon at Fraunhofer ISE using a RTCVD system designed to offer the technical potential to be convertible to a continuously operating system [79]. Growth rates of up to 10μm/min have been demonstrated. An efficiency of 8.0% and a V_{oc} of 553mV has been achieved on RTCVD epitaxial layers deposited with this system on SSP ribbons [80]. An efficiency of 13.2% and a V_{oc} of 614mV has also been achieved on heavily doped mc-Si with this system [2]. The diffusion length was 8.5–12μm for a cell thickness of about 10μm. IMEC and KU Leuven have achieved an efficiency of 7.6% using CVD layers on SSP pre-ribbon with MIRP hydrogenation [81].

4.2.3 Silicon on Diffusion Barriers

If a diffusion barrier is deposited between the active layer and a low-cost substrate, then diffusion of impurities from the substrate into the active layer can be reduced. The diffusion barrier properties of SiO_2 (deposited by PECVD) have been investigated at Fraunhofer ISE [82]. Iron was used as the introduced impurity because it is fast-diffusing and can significantly reduce minority carrier lifetimes. It was shown qualitatively that SiO_2 of 0.5 to 4μm thickness is a good diffusion barrier against iron at temperatures of 1000–1400°C with typical solar cell process times.

It is important to achieve low recombination rates at the silicon/diffusion barrier interface. One way of doing this is to dope the diffusion barrier with boron.

Porous silicon has been used as an intermediate layer for growth on low quality silicon substrates [83]. It was found that the porous silicon acts as a diffusion barrier and getters impurities from the substrate. Porous silicon also acts as a back side reflector, which is otherwise difficult to achieve with a silicon substrate. In order to achieve reasonable epitaxial quality, deposition temperatures were limited to 800°C.

Silicon deposited onto diffusion barriers (other than porous silicon) without recrystallisation tends to have a small grain size. Delft Univerisity of Technology found silicon deposited on SiO_2 by CVD with or without a LPCVD nucleation layer had average grain sizes of 1–2μm [84].

Recrystallisation is often used to increase grain size and improve electrical properties. Mitsubishi Electric Corporation have produced a 4cm^2 cell of 16.4% efficiency and V_{oc} of 608mV [85] (not confirmed

independently) and a 100cm^2 cell of 14.2% efficiency [86] (confirmed independently) by ZMR and CVD on SiO_2. LPCVD was used to deposit 3–5μm of μc-Si on SiO_2 grown on c-Si substrates. Capping layers of SiO_2 and Si_3N_4 were deposited and ZMR was applied. The capping layers were etched away and a BSF layer followed by the active layer were deposited by CVD to a thickness of about 60μm. The c-Si substrate and rear SiO_2 were removed to allow contact to the rear of the cell, except for a grid which was left unetched to provide mechanical stability. H^+ ion implantation from the rear was used for defect passivation and an oxide was used for front passivation. It was found that hydrogen passivation increased cell efficiency by a factor of 20–30% [87]. The influence of the ZMR scanning speed was investigated by varying it from 0.2–1mm/s. Defect densities were 2×10^6cm^{-2} at 0.2mm/s and 3×10^7cm^{-2} at 1mm/s. It was found that the (100) orientation dominates at low scan speeds so anisotropic etching can be used for texturing to form random pyramids. An AR coating was used to further improve light confinement. Diffusion lengths of up to 150μm were achieved with low scanning speeds and H^+ passivation. It has been found that the scanning speed can be increased to 3mm/s with good results if the seeding layer is thinner (0.5μm) [88]. Fine temperature control of the ZMR has also been shown to be important in achieving low defect densities [89]. A later development of this technology is to etch via holes through the grown layer and dissolve the SiO_2 with HF, allowing detachment of the grown layer and recycling of the substrate (see section 5.2).

Promising results have also been achieved in a collaboration between IMEC and Fraunhofer ISE [90]. The process involves deposition of SiO_2 on sc-Si, followed by chemical vapour deposition of a seeding layer and a capping layer of SiO_2, ZMR, phosphorus gettering and etch-back, and deposition of the active layer. A dry cell process developed by Fraunhofer ISE produced a cell of 9.3% efficiency on a layer with a B-doped initial SiO_2 layer. An interdigitated IMEC process without an AR coating resulted in a cell of 4.8% efficiency on a 30μm thick layer. Surface roughness (2–3μm) caused problems which was solved by mechanical polishing for the Fraunhofer cells and a different resist spinning procedure for the IMEC cells. Diffusion lengths of 12–17μm were achieved. It was found that intra-grain recombination dominates performance in these cells. An efficiency of 12.8% has been achieved with a non-dry cell process which included texturing and hydrogen passivation [91]. The same process on SSP substrates produced from semiconductor grade silicon powder resulted in an efficiency of 10.4% for a 1cm^2 cell. SSP substrates made from low-cost Si powder were too rough to undergo ZMR without a surface smoothing treatment.

The advantages of bare silicon and silicon which has been coated with a diffusion barrier can be combined to some extent by using a substrate which provides a partial epitaxial template and a partial diffusion barrier. A perforated SiO_2 barrier on a silicon substrate has been investigated at Fraunhofer ISE. SiO_2 was deposited on SSP ribbon, the SiO_2 layer was perforated with a lithographic process, and an epitaxial RTCVD seeding layer was deposited, as shown in figure 3 [92]. This layer was then recrystallised by large area melting and the active layer was grown on top. The perforation (seeding) holes were 250μm in diameter on a 2.5mm grid ie. they covered about 1% of the surface. Grain size after recrystallisation is determined by the distance between the seeding holes, which was about 2.5mm. The cell process included remote plasma hydrogenation to achieve an efficiency of 11.5% and a V_{oc} of 562mV with an effective diffusion length of 35–70μm for an active layer thickness of 50μm.

A variant of this approach is epitaxial lateral overgrowth (ELO). Silicon is grown epitaxially out of seeding holes in a barrier layer (usually SiO_2). The silicon overgrows the barrier layer and if a pattern of seeding holes is used, closed layers can be achieved. ELO utilises the large differences in growth rates of different crystal orientations achievable on silicon. Width to height ratios for single crystal epitaxial layers grown by this technique can be as high as 40:1 for substrates slightly misoriented from $\langle 111 \rangle$ [93]. Growth is perfomed near thermal equilibrium so that silicon is not deposited directly on the barrier layer. Epitaxial lateral overgrowth for solar cells has been investigated at the University of Delaware using LPE over SiO_2

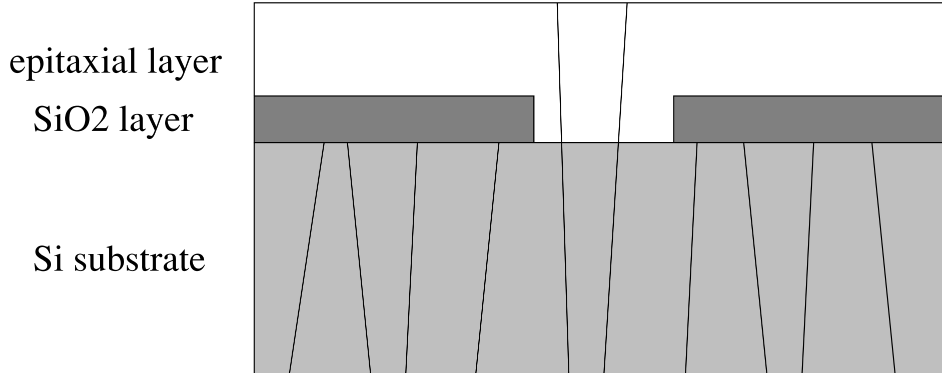

Figure 3: Cross section of the epitaxial layer, perforated SiO_2 barrier and SSP substrate structure produced at Fraunhofer ISE.

on highly doped sc-Si substrates [94]. The aim is for the interlayer to eventually be both reflecting and passivating. The active layer/SiO_2 interface has a reflectivity of about 40%. The level of passivation provided when silicon overgrows SiO_2 is unknown but it will need to be large if high efficiencies are to be achieved. Epitaxial lateral overgrowth by CVD has been investigated at Delft University of Technology [84]. SiO_2 lines 2μm wide covering 50% of the wafer area were obtained by lithography. Growth was epitaxial but many twins were observed over the SiO_2 regions.

Beijing Solar Energy Research Institute has used RTCVD to deposit silicon on c-Si p^{++} substrates with perforated SiO_2 or Si_3N_4 interlayers [67]. Better morphology was found on layers grown on Si_3N_4, possibly because the Si tended to ball up on the SiO_2 and create gaps between the grains. The grain orientation was preferentially $\langle 100 \rangle$ on SiO_2 and $\langle 111 \rangle$ on Si_3N_4.

RF PECVD has been used to grow μc-Si at 0.12μm/min on bare and SiO_2-covered c-Si at Saitama University. [95] [96]. The effect of the surface roughness of SiO_2 was investigated and it was found that crystallinity was improved by a moderately roughened SiO_2 surface.

Deposition of silicon by PECVD on Si, SiO_2 and quartz has been investigated at Kyoto University with temperatures of 500–900°C [97]. Film thickness were 0.5–3μm with growth rates of 5–40nm/min. Films on SiO_2 had a very strong (110) orientation at 900°C. It was found that films were amorphous below 600°C and that crystallinity improved as the temperature increased. Between 600 and 800°C films were partly polycrystalline and above about 800°C films were totally polycrystalline.

A large range of grain sizes introduces nonuniformities in the minority carrier diffusion length which can result in a cell whose performance is dominated by poor quality regions. One way to address this is to control the location of nucleation sites. Canon have introduced a selective nucleation-based epitaxy process (SENTAXY) [98]. This involves the use of artificial nucleation sites to control the size of crystallites and their boundaries. SiO_2 on sc-Si is irradiated with silicon ions to form a lattice of silicon-rich SiO_2 points which behave as artificial nucleation sites. Silicon is then deposited by CVD. Islands of SiN_x in SiO_2 have also been used to provide artificial nucleation sites. Canon have also developed a low-temperature SENTAXY technique.

4.3 Summary of Silicon on Silicon

Institution	**Substrate**	**Deposition Method**	**Electrical**	**Refs**
		Single Crystal Substrates		
ANU	p-type sc-Si	LPE & substrate thinning	18%, 666mV	[63]
UNSW	p^+ sc-Si	CVD	17.6%, 664mV	[66]
Fraunhofer ISE	p^+ sc-Si	RTCVD	17.6%	[2]
MPI-F	sc-Si	CVD	17.3%, 661mV	[60]
ANU	p^+ sc-Si	LPE & substrate thinning	17%, 651mV	[64]
UNSW	p^+ sc-Si	LPE	16.4%, 645mV	[65]
ASE GmbH	p^+ sc-Si	CVD	15.4%, 623mV	[61]
IMEC	p^+ sc-Si	CVD	14.9%, 635mV	[57]
MPI-F	p^+ sc-Si	LPE	14.7%, 659mV	[62]
Beijing SERI	p^+ sc-Si	RTCVD	12.1%, 626mV	[67]
		Mc-Si, ribbon and MG-Si Substrates		
ANU	p-type mc-Si	LPE	15.4%, 639mV	[70]
ANU	p^+ mc-Si	LPE	15.2%, 639mV	[70]
IMEC & KU Leuven	p^+ mc-Si	APCVD	13.3%, 615mV	[71]
Fraunhofer ISE	p^+ mc-Si	RTCVD	13.2%, 614mV	[2]
IMEC	p^+ mc-Si	CVD & industrial cell process	12.1%	[73]
IMEC, KU Leuven & Bayer	RGS-ribbons	CVD	10.4%, 558mV	[77]
Fraunhofer ISE	SSP ribbons	RTCVD	8.0%, 553mV	[80]
IMEC & KU Leuven	SSP pre-ribbons	CVD	7.6%	[81]
I Kristallzüchtung	mc-Si	Temp diff LPE	τ = 5–10μs	[9]
NREL	MG-Si	LPE	L = 42μm	[75][76]
		Substrates with Diffusion Barriers		
Mitsubishi Electric	SiO_2 on Si	ZMR & CVD	16.4%, 608mV	[85]
Franhofer ISE	SiO_2 (perforated) on SSP-Si	RTCVD & large area heating	11.5%, 562mV	[92]
IMEC & Fraunhofer ISE	SiO_2 on Si	ZMR & CVD	9.3%, 529mV	[90]
Frauhofer ISE	SiO_2 on Si	LPCVD & ZMR	6.1%	[99]
Delft UT	SiO_2 on Si	CVD	grain size 1–2μm	[84]

5 Lift-off silicon layers

5.1 Introduction

Thin film silicon layers which can be detached from a reusable silicon substrate have a very high efficiency potential. This is mainly due to the fact that as the substrate is recycled, there is no need to compromise on material quality. In addition, the inherent disadvantages of deposition on non-silicon substrates such as diffusion of impurities, material defects and film stresses are absent [100]. The radiation tolerances of these thin film cells may be very high because large amounts of damage can be sustained before the diffusion length falls to less than the wafer thickness.

Most of the groups working in this area grow single crystal silicon on a high quality substrate with a sacrificial attachment region. This region may be of a different doping level, made from porous silicon or made from SiO_2. A disadvantage of using doping levels and dopant selective etchants is that high temperatures may broaden doping profiles. A porous silicon sacrificial layer allows epitaxy, bonding and oxidation to occur at higher temperatures. Porous silicon also has a very high etch selectivity over non-porous silicon; ratios of up to 10^5 have been demonstrated [101]. For growth processes which use hydrogen, less hydrogen is used in the growth of sc-Si, compared with the case of non sc-Si during which hydrogen is used to passivate grain boundaries [102].

Groups who are working on detachable layers include Mitsubishi Electric Corporation, Canon, Sony Corporation, two German groups centered in Erlangen and at the University of Stuttgart, the Australian National University, Silicon on Insulator Technology (SOITEC), LPM and Canon. With the exception of Canon, the groups detailed here aim to recycle the substrate.

5.2 VEST process - Mitsubishi Electric Corporation

A 77μm thick cell with an area of 96cm^2, an efficiency of 16% and a V_{oc} of 589mV has been achieved using the VEST (etching of underlying substrate through via-holes in the silicon film) process at Mitsubishi Electric Corporation [100] [103]. Mitsubishi have also demonstrated the reliability of their technique. From a batch of cells of 10cm^2 area, 22 of 25 had an efficiency greater than 15% [100]. A 13.1% efficient module of 924cm^2 has also been demonstrated [104].

VEST cells are made by first separating the active layer from the substrate and then fabricating a cell. Figure 4 shows the VEST cell structure. Layer separation is achieved by forming a silicon on insulator (SOI) layer on SiO_2 deposited on a c-Si wafer. A thin seeding layer of silicon is deposited by CVD with a capping layer. This is followed by zone melt recrystallisation (ZMR). The resulting silicon is mainly (100) orientated. A back surface field and thick active layer is then deposited by CVD. An anisotropic etch through a masking layer is used to form an array of 100μm^2 via holes through the silicon layer to the underlying SiO_2. The hole spacing is 1.5mm. The SiO_2 layer is then removed with HF which enters through the via holes, causing layer separation. Cell fabrication is preceded by another anisotropic etch which forms random pyramids on the front surface.

Cell fabrication involves a phosphorous diffusion to form a heavily n-type region over the entire surface and down the via holes, an etch back of the front surface to form the emitter and application of a SiN antireflection coating using LPCVD. The final steps are formation of an interdigitated pattern of n and p regions on the rear surface, screen printing of both base and emitter electrodes on the rear and implantation of hydrogen ions for passivation. Recently, a plasma CVD process has been used to provide both hydrogen passivation and an ARC [104]. The electrodes are made of a paste which is screen printed directly onto the cell. For the emitter it is an Ag paste and for the base, an Al containing Ag paste [103].

A feature of the VEST technique is that the ZMR process results in a mostly (100) surface orientation which allows texturing. Finger shading losses can be avoided since both electrodes are on the

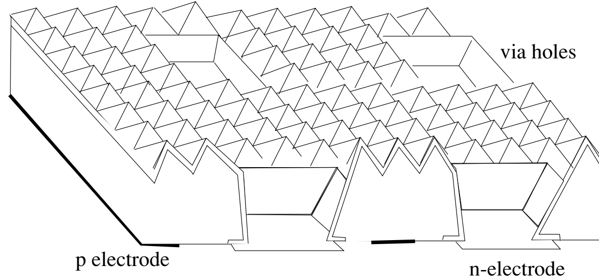

Figure 4: Schematic of the VEST cells, after Morikawa [103]

rear and current is collected from the sunward surface through the via holes. The c-Si substrate may be recycled [100].

The VEST cell fabrication technique has been optimised to overcome a number of difficulties. The diffusion length, L_{diff} after ZMR is quite low (40μm) and this has been increased to 167μm by phosphorous gettering and etch back. There is a decrease in fill factor caused by the high series resistance of the emitter since both contacts are on the rear and the via holes are widely spaced. This has been partially overcome by arranging for a heavy phosphorous diffusion in the via holes and a lighter diffusion on the top surface. The top surface diffusion is $60\Omega/\square$ which results in a significant loss of blue response. A drawback of the VEST technique is that at present the electrodes are formed by a screen printing process, which requires a minimum film thickness of about 80μm [100].

5.3 Sony Corporation

Sony Corporation have used a sacrificial porous silicon layer and have achieved a 12μm thick, thin film cell of 4.0cm^2 area, with an efficiency of 12.5% and V_{oc} of 623mV [105]. A material lifetime of 60μs has been demonstrated.

Sony cells are made by first anodising a silicon substrate. Three porous silicon layers are formed, two of low porosity (16% top layer and 26% bottom layer) and one of high porosity (40–70%). The location of the high porosity layer is shown in figure 5 and its function is to allow easy separation of the cell layer from the substrate. The crystalline structure and pore distribution of the porous silicon are altered by a high temperature hydrogen anneal at 1100°C for 30 minutes. This causes the low porosity layer to form small, circular pores while the high porosity layer tends to form broad based pillars and wide voids. During this anneal, the porous layer also acts to getter metals. Epitaxial growth of the active silicon layer occurs directly onto the top surface of the substrate and as this is of low porosity, the grown layer has a low lattice strain. A 1μm thick p^+ layer is grown epitaxially onto the substrate, using silane and hydrogen diluted B_2H_6 gas at atmospheric pressure. This is followed by the growth of an 11μm thick p-layer which forms the base region of the solar cell. Phosphorous diffusion, application of a TiO_2 antireflection coating and metallisation completes the cell. Layer separation is achieved by the application of a weak tensile stress or ultrasound. The porous layer is then removed and the substrate can be recycled [105].

The 12.5% efficient cell had an oxidation step which served to passivate the front surface and a TiO_x antireflection coating. An inexpensive plastic film was adhered to the front surface for mechanical strength.

A minor disadvantage of the process developed at Sony is that the porous layer is 8μm thick at present and this is sacrificed in cell production. A planned improvement is to put an optical reflector on the rear of the cell [105].

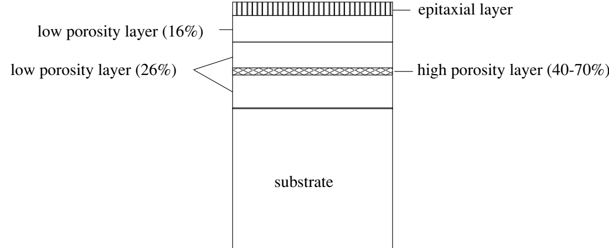

Figure 5: Structure of the substrate, porous silicon and epitaxial layers of the Sony cells, after Tayanaka [105]

5.4 Ψ process / QMS

The Perforated Silicon (Ψ) process developed by a consortium of German groups is very similar to the technique used at Sony. There are now two distinct groups working with this material. Waffle cells have been developed in Erlangen and have shown a lifetime of 0.27μs and L_{diff} of 11μm on a 5.8μm thick layer [106]. A cell efficiency of 4.4% (501mV) has been reported for a 7μm thick cell transfered to a glass substrate [107]. Quasimonocrystalline silicon (QMS) has been developed at the University of Stuttgart and has been used to demonstrate a cell efficiency of 10.3% (601mV), for a 49μm thick layer, on a 3.9cm^2 cell area [108].

The first step in the Ψ process is the texturing of the surface of a sc-Si substrate using a combination of photolithography and KOH etching. Two distinct porous silicon layers (PSL) are then formed on the substrate using an anodic etch in HF solution. The upper layer is about 30% porous and the bottom about 50%. The PSL are stabilised by an oxidation step. Prior to epitaxy, the sample is heated to 850°C for around 10 minutes to remove the native oxide which forms on the porous silicon. To make waffle cells, a layer of silicon is deposited using ion assisted deposition (IAD) at a substrate temperature of 700°C. Deposition rates of 1Å/s have been achieved [108]. The deposited film has the same crystallographic structure as the substrate. A low temperature deposition technique is advantageous since at temperatures greater than 850°C, sintering of the porous silicon occurs due to the surface mobility of silicon atoms on the inner surface. Once cell fabrication is complete, the layer can be separated from the substrate using mechanical stress. This is done by attaching a glass superstrate to the front surface with a transparent encapsulate (poly-ethylenphtalate). Further steps, such as surface passivation and reflector formation on the rear surface, must occur below a temperature which both the encapsulate and superstrate can withstand. Earlier versions of the Ψ cells, which did not have the two porosity levels, were removed by a 2 minute ultrasonic agitation. The rear surface is then passivated and a reflector added. After the PSL is removed, the substrate can be reused several times before retexturing [102] [106]. Future improvements which are planned include a reduction in the porous layer thickness (which is currently 10–15μm thick [109]) and an increase in the deposition rate [102] [106].

Work on the Ψ process to produce waffle cells has been done by a collaboration of groups centered in Erlangen. The films are termed waffle due to the three dimensional texturing of the entire film. The optimum period of texturing for effective light trapping (and reflection control) has been theoretically determined to be about the same as the waffle thickness. Layers of 85mm in diameter have been separated from the substrate using mechanical stress. A feature of this technique is that the emitter is grown epitaxially, since this is faster than diffusion. A 7.8μm thick, pyramidal structure with a dislocation density less than 10^4/cm^2 has been formed [102].

IPE, Universität Stuttgart, have termed the silicon quasimonoscrystalline silicon (QMS) due to the high density of voids [108] [110]. The 10.3% efficient cell was reported at IPE where CVD, rather than

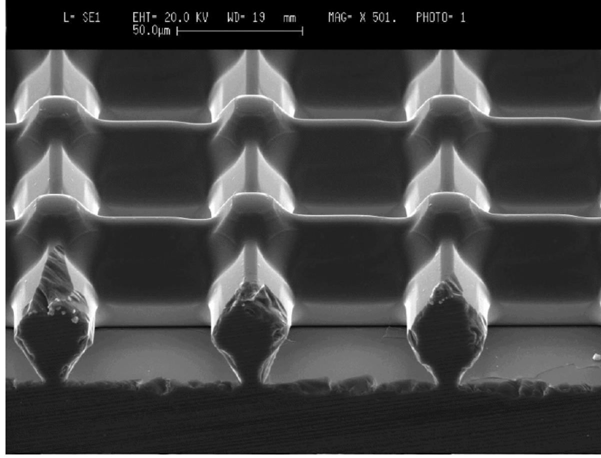

Figure 6: The epilift structure. The epilayer is still attached to the substrate and the diamond cross section of the layer is visible.

IAD has been used and the deposition temperature is much higher (1100°C, compared with 700°C). Layer thickness is 12–50μm and consists of an initial back surface field layer, followed by an absorber layer. The front grid is formed using photolithography and a SiN_x ARC is used. Separation of the layer is by mechanical force after attaching it to glass using an organic resin. Modelling has been done which shows that a 25μm thick layer with a L_{diff} of 40μm may lead to a 17% cell [108] [110].

5.5 Epilift process - Centre for Sustainable Energy Systems, ANU

At the Centre for Sustainable Energy Systems, ANU, the epilift process has been used to grow layers of 50–100μm thickness on single crystal silicon. A lifetime of 3.8–11.7μs for a sample with a light phosphorous diffusion and thin oxide as surface passivation has been achieved [111].

The epilift process involves deposition and patterning of a masking layer on a sc-Si substrate. The masking layer is exposed in a mesh pattern; lines are of 2–10μm width and spaced 50–100μm apart. The substrate is usually orientated in the (100) direction, the mesh in (110) directions. An epitaxial layer is grown on the substrate using liquid phase epitaxy (LPE). The growth faces have mostly (111) orientation and the layer has a diamond cross section, giving it a natural antireflection texture. Initially deposited layers are more heavily doped (which means they are etched faster) and later layers more lightly doped. A selective etch is used to remove the epilayer. The masking layer and substrate may be reused provided the masking layer is not attacked by the etch. Figure 6 shows an SEM image of the epilayer structure attached to a substrate [111] [112].

The epilift layer grows in a mesh pattern and the holes can be closed over to an arbitrary amount. An advantage of the holes is that they allow both contacts to be on the rear, thereby avoiding shading losses. A possibility for cell fabrication is to leave the epilayer partially attached to the substrate (for example, at the corners) and to process the cell, attach the epilayer to a superstrate and then detach the cell from the substrate [112].

An indium solvent is used in the growth of epilayers, and films with an area of 10cm^2 and a thickness of up to 100μm have been detached. A film without holes was achieved by leaving an epilayer attached only at the corners, growing again and using shear force to separate the layer. A potential problem with the technique is that the material may have a high dislocation density [112]. The dislocations are due to the oxide mask used and are not evenly distributed across the wafer [111]. Cell efficiencies achieved by this process have not been reported.

5.6 Smart Cut - SOITEC

'Smart Cut' technology has been introduced at Laboratoire d'Electronique de Technologie et d'Instrumentation (LETI) and co-developed with SOITEC (Silicon on Insulator Technology). The technique provides a method for separating a thin layer of silicon from a bulk wafer [113]. At present it is mainly in use in the IC industry, although it has applications for solar cells [114]. The technique involves growing a SiO_2 layer, and implanting hydrogen into the silicon underneath this layer. Most of the hydrogen atoms come to rest some distance below the silicon/SiO_2 interface, creating a mechanically weakened layer. By bonding the SiO_2 layer to a silicon wafer or a quartz or glass superstrate, a thin (200nm) layer of silicon can be peeled from the original wafer [113] [114]. When a silicon wafer is used as the superstrate, separation is achieved using a heat treatment at 400–600°C. A second heat treatment at more than 1000°C is used to strengthen the chemical bonds between the superstrate and the thin silicon layer. The substrate wafer can then be polished and is ready for hydrogen implantation and reuse [113]. An advantage of the technique is that the silicon layer has low defect levels which are close to those of bulk silicon [115].

Since the separated layer is very thin (200nm [115]) epitaxial growth of a thicker active layer of silicon must take place after separation of the seeding layer from the substrate. A supporting superstrate that has a thermal expansion coefficient similar to silicon will be needed. A number of options exist for such a substrate, such as an oxidised silicon wafer with pre-existing holes at a 1mm spacing. Separation of this wafer from the epitaxially grown layer would simply require immersion in hydrofluoric acid (HF). There is some concern about the cost of hydrogen implantation.

5.7 Eltran Process - Canon Incorporated

A technique termed ELTRAN (epitaxial layer transfer) has been developed by Canon. This is based on a new BESOI (bond and etch back of silicon on insulator) technology [101]. An epitaxial layer is formed on a 10μm thick porous silicon layer by chemical vapour deposition (CVD) at 1000–1150°C and the rear of the surface is exposed by grinding away the original wafer. The porous silicon can then be removed. An etchant selectivity of 10^5 has been achieved [101]. At present, the fact that the substrate wafer is destroyed makes this process inapplicable for solar cell technology. However, in future the technique may be adapted for photovoltaic applications.

5.8 LPM - CNRS

A group from LPM-CNRS have formed epitaxially grown thin film layers of 25μm thickness. The method involves direct texturing of sc-Si, grid formation and LPE growth. The grid is formed by patterning and electrochemical etching of the substrate. Growth is done by LPE with the grid either attached or detached. It is intended to eventually transfer the grid to another substrate, for example, mullite ($Al_6Si_2O_{13}$) [116].

5.9 Summary of lift-off silicon layers

Group/Technique	Thickness	Result	Comment	Reference
Mitsubishi, VEST	77μm	16%, 589mV	poly-Si layer	[100] [103]
Sony Corporation	12μm	12.5%, 623mV	plastic superstrate	[105]
Waffle cells	5–8μm	4.4% (501mV)	waffle cell	[102] [106] [107]
QMS	49μm	10.3%, 601mV		[108] [110]
Epilift, ANU	50–100μm	3.8–11.7μm(τ)		[111] [112]
Smart Cut	200nm		method of slicing wafers	[113] [114] [115]
Canon			substrate is destroyed	[101]
LPM	25μm			[116]

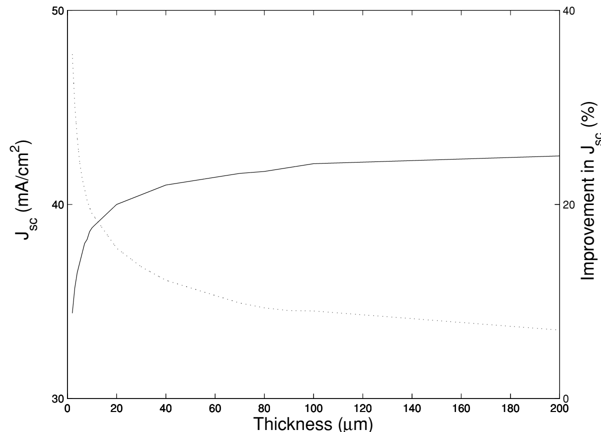

Figure 7: This graph shows the percentage improvement in J_{sc} (right axis, dotted line) which can be achieved by having a lambertian, rather than polished, front surface as a function of cell thickness and the J_{sc} obtained using a lambertian surface as a function of thickness (left axis, solid line). After Campbell and Green [117].

6 Light Trapping

6.1 Introduction

Light trapping is especially pertinent for silicon cells due to the low absorption constant in the infra red region. As cell thickness decreases, the maximum attainable J_{sc} drops sharply and the improvement which may be attained with a lambertian surface (compared with a polished surface) increases substantially [117]. Hence light trapping is vital to achieve high efficiencies for thin film cells. Fortunately, the nature of most thin film depositions is such that the surface is far from optically flat and hence some degree of light trapping is inherent. In many instances, additional measures may be taken and light trapping schemes developed for conventional silicon solar cells are not always applicable to thin cells. In particular, direct texturing of a thin film may be too damaging [118]. For thin film silicon on foreign substrates or cheap silicon substrates, the crystallographic orientation is often random. In this case, anisotropic etching may be too unreliable and photolithography too expensive [118]. Similarly, texturing of a silicon substrate is undesirable as it may lead to an increased number of nucleation sites and therefore a lower quality material [118]. Alternative techniques developed for thin film light trapping schemes include a textured substrate or deposition of a textured layer onto a substrate prior to growth of a thin film layer. Thorp has claimed that for thin films, antireflection properties may be as important as light trapping properties [118].

Figure 7 is adapted from Campbell and Green [117] and shows the improvement in J_{sc} which may be obtained using Lambertian, rather than polished, surfaces as a function of cell thickness and the maximum attainable J_{sc} as a function of cell thickness. Cell thicknesses may not be simply read from this graph for cells deposited on textured substrates, as the effective width and the thickness of the deposited layer will not be equal.

Light trapping achievements are usually measured in terms of improvement in the short circuit current. It should be kept in mind that J_{sc} is also affected by surface recombination and minority carrier lifetime. Light trapping is related to the extra absorption achieved due to the light trapping structure. This is dependent on surface texturing and internal reflectivity of the front and back surfaces [119].

An issue which has arisen when considering light trapping in thin film cells is the relationship between texture period and cell thickness. For conventional cells, the texture period has always been much less than the thickness [120]. Textured substrates and thin films allow the effect of a texture period much

greater than the thickness to be investigated [121]. A texture period in the range of microns is necessary to investigate the effect of having a texture period in the same order of magnitude as the film thickness, this has been demonstrated with the sol gel coating developed by several groups based in Germany.

6.2 Textured silicon surface

Deposition of silicon onto foreign substrates often results in a naturally occuring surface texture and Kaneka have used this to advantage in the STAR cells (naturally surface texture and enhanced back reflector) [122], [123]. The surface texture of STAR cells is controlled primarily by the deposition temperature but also by deposition rate, the ELA (excimer laser anneal) conditions and the surface treatment of the laser annealed poly-Si [122], [123]. STAR cells have demonstrated a very high J_{sc}.

6.3 Textured substrates

An alternative to direct texturing of a silicon film is to texture the substrate. This is being investigated by a number of groups. The simplest textured surfaces are two dimensional grooves although three dimensional texturing is more effective. Another possibility is random texturing.

Two dimensional texturing to date has used conformal grooves. In addition to their light trapping properties, conformal grooves lead to an increased surface area, which may allow for better heat transfer. A disadvantage of the conformal grooves is that the increased cell volume leads to increased recombination and therefore to losses in V_{oc} [124], this is also the case for three dimensional texturing. Most modelling results have predicted values for J_{sc} of around 35mA/cm^2 for cell thicknesses of about 5μm when using a V-grooved substrate.

Encapsulated-V texturing has been demonstrated and modelled at the Max-Planck-Institut für Festkörperforschung. The encapsulated-V texture is formed by mechanically texturing a glass surface with V shaped grooves. Silicon is then deposited by ion-assisted deposition. The substrate temperature is 610–650°C. A detached back surface reflector (BSR) and shallow groove angles corresponding to a texture period of 500μm on the glass were used. Having the BSR detached acts to decrease the number of reflections and therefore light absorption in the BSR. An additional advantage of the BSR is that it is made from aluminium and so may provide series connection [125].

Three dimensional texturing of foreign substrates may be realised by imprintation of ceramic substrates while in powder form and by embossing micron sized features in glass substrates [121].

A pyramidal film texture has been developed by groups at Max-Planck-Institut für Festkörperforschung and the Universität Erlangen. Theoretical predictions are for a J_{sc} of 37mA/cm^2, assuming a thickness of 4μm, a texture period of 15μm and a facet angle of 75°. A texture period of 500μm is more in line with what is achievable today and results in a J_{sc} of 34mA/cm^2. Facet angles between 0 and 80° were modelled and cell performance was found to increase with increasing facet angle [126].

Foreign substrates may lend themselves more readily to random texturing than to regular texturing. A randomly textured substrate allows the lambertian limit to be approached.

Surface scattering is said to be responsible for the efficiency of 7% and J_{sc} of more than 25mA/cm^2 on the μc-Si:H cells deposited on glass substrates at the Academy of Sciences of the Czech Republic and the Universite de Neuchatel [127].

6.4 Substrate coatings

Max-Planck-Institut für Festkörperforschung, the Institut für Neue Materialien and the Universität Stuttgart have collaborated to investigate the possibility of using a sol-gel coating on a glass substrate. The sol is made from tetraethoxysilan, trimethoxysilan and silica sol using a hydrochloric acid catalyst. It sets to

form a gel film. The aim is to provide surface texturing which has a period in the same order of magnitude as the film thickness [120]. Theoretical modelling has been used to determine the relative advantages of 4 different features; encapsulated-V texture with a V-grooved glass substrate, tripyramidal film, square pyramidal film and hexapyramidal film. All features have advantages of large facet angles which reduces reflectance. The BSR is detached from the silicon layer to reduce reflections. Both the air/glass and glass/silicon interfaces are without antireflection coatings. The modelled thickness was 4μm and each cell included a SiO_2 layer for surface passivation at the silicon/air interface. (SiO_2 also provides some antireflection properties) [120].

Using the 3-dimensional textures, the J_{sc} value was generally larger and an average path length of 49 times W_{eff} was obtained. 2-dimensional textures resulted in an average path length of 12 times W_{eff} [120]. The efficiency of thin cells was found to be current, rather than voltage controlled and texturing almost doubles the current. The theoretical best value for J_{sc} was 40mA/cm^2 which was achieved with a thickness of 4μm, a facet angle of 75 degrees and period of 15μm. The front glass surface was textured (grooves).

Preliminary sol gel textured surfaces have been prepared. Facet angles were 40° at ridges, decreasing to 0° at the base of the pyramids. The embossing process has not yet been optimised and initial films did not hold their shape. Sol gel substrates will require a deposition temperature of less than 500°C to prevent decomposition of the film.

Other substrate coatings which have been investigated include ZnO on glass or stainless steel and a diffraction grating. ZnO may be applied using magnetron sputtering. The deposited layer can then be chemically etched [128] [129]. Sony are investigating the use of a diffraction grating on both the rear and front surface of a cell [130].

6.5 Porous silicon

Porous silicon may be useful for light trapping of thin film cells, having the ability to diffuse light well [131], although the electrical transport properties are not yet fully understood [132]. Porous silicon is formed using electrochemical anodisation [131] and the porosity level controlled by varying the current density. The process is usually quick, but requires handling of single wafers [133]. The refractive index of silicon decreases with increasing porosity [134] [135], and varies from 1.7–2.1 [136]. The large surface area of porous silicon samples means that good surface passivation techniques will be necessary [131]. The fact that porous silicon absorbs a fair amount of light will need to be addressed [136]. The structure of porous silicon is sensitive to high temperatures such that any further processing steps may need to be done at lower temperatures [131]. The reliability of porous silicon over time also needs to be investigated [136].

At IMEC, the use of porous silicon as a diffuse backside reflector has been investigated [131]. Epitaxial layers of 2–3μm have been grown on porous silicon layers of about 350nm. The resulting layers were of lower reflectance but highly defected, and consequently a low quality material [131].

The use of a porous silicon multilayer for a backside reflector (BSR) has been investigated by a cooperation of groups centred at the Bavarian Centre for Applied Energy Research [134] [135]. A highly doped substrate is used, and a porous layer formed on this by anodic etching. A thin film silicon layer is then grown on the porous silicon layer. Advantages of the process are that it is simple, fast and compatible with standard cell processing. It is also conceivable to combine light trapping with back surface passivation if the porous silicon layer has a thin p^+ layer grown into it. A challenge for the group is to grow epitaxially on the porous silicon and still maintain the reflectance capabilities of the porous silicon. Maximum reflectance occurs if a large number of porous layers are stacked. Bragg reflectors are formed by stacking layers with alternating porosity such that $nd = \lambda/4$ [135]. At present, 20 layers are used with porosities alternating between 0.4 and 0.6 and layer thicknesses of 125nm and 100nm respectively [135]. A cell was made such that porous silicon covered one half of the surface. An epitaxial layer was grown on both the porous silicon

layer and on the bare silicon area. The epitaxial layer was a 3μm p-type silicon layer deposited by CVD at 1000°C. The result was an increase in EQE for all wavelengths in the range 350–1000nm but it is possible sintering of the porous silicon layer caused an increase in epilayer thickness. The reflectance was enhanced in the 900–1100nm range [134]. The value of J_{sc} was 9mA/cm^2 and 12.5mA/cm^2 for layers grown on bare silicon and on porous silicon respectively. No ARC was used [135].

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